EREC G5 Stage 2 Sub-group

Meeting No. 6

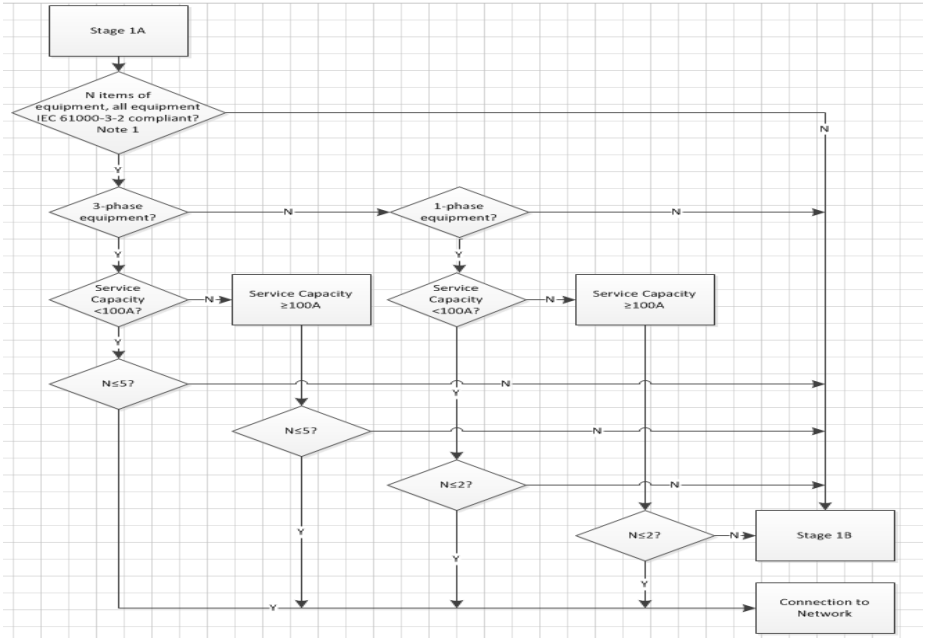
Held at ABB Office, Warrington WA4 4BT

On Wednesday 30th November 2016 10:00-15:00

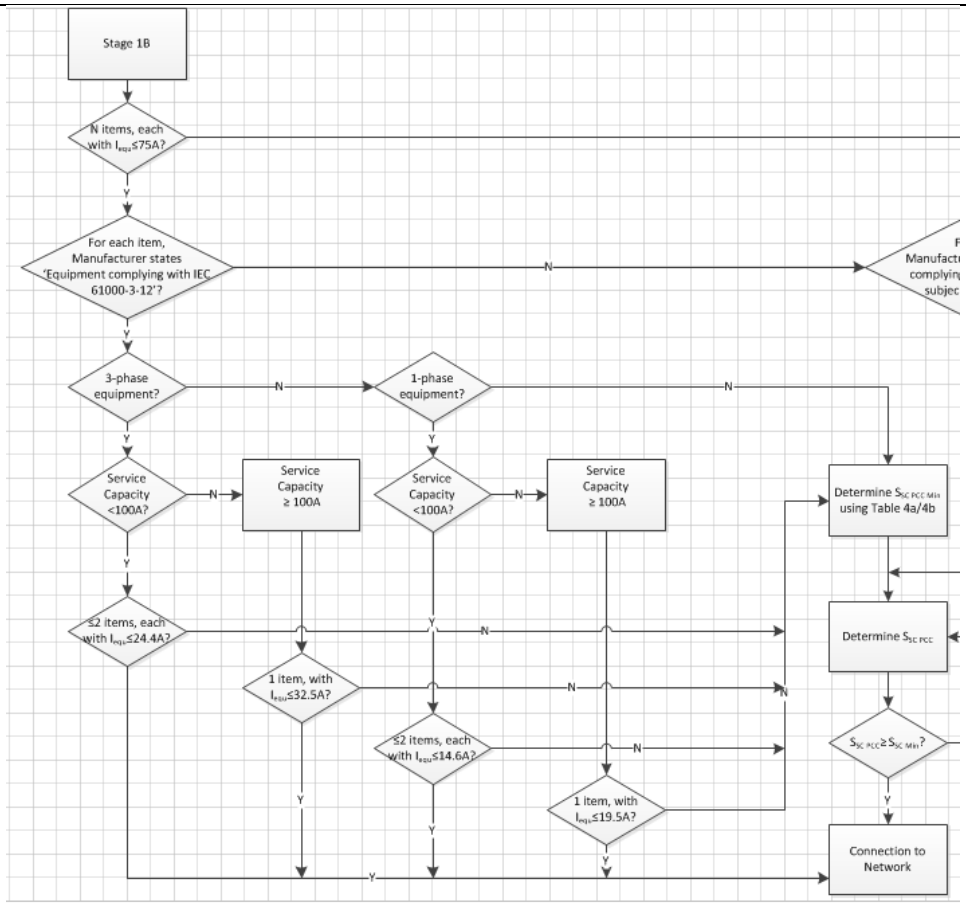
Meeting Notes

Attendee	**Affiliation**	**Initials**	**Role**
Frank Griffiths	ABB	FG	Member
Andrew Oliver	TNEI	AO	Member
Simon Scarbro	WPD	SPS	Chair
Ahmed Shafiu	Siemens	AS	Secretary
Apologies	**Affiliation**	**Initials**	**Role**
Ben Gomersall	National Grid	BG	Member
Forooz Ghassemi	National Grid	FGh	Member

Item	**Topic & Note**	**Action**
2.	**Agree Notes of Previous Meeting** Agreed.	
3.	**Actions from Meeting 3**	
3.1	**Definition of Converter Types** SPS showed the revised composite draft text. AS to check this with Siemens' technical specialists.	AS
3.2	**Harmonic Impedance of LV Networks** At SPS's request, AO had done some modelling in IPSA to explore the various recommended models and their impact on the harmonic impedance versus frequency of LV networks. It is clear that the key factor is the capacitance connected to the LV network which gives a parallel resonance. It is expected that networks will vary in this respect. Recommended values differ widely. It was agreed that we would stick with the present k-values for LV. It was agreed that SPS would highlight to the full WG that it would be useful to instigate harmonic impedance measurement of sample networks. This may not fit with the delivery timescales for the revision.	SPS
4	**Stage 1 & 2 Draft**	
4.1	**Impact of Siemens Emission Data & (BS) IEC 10002-6** It was agreed that we ignore the (BS) IEC 10002-6 values. The Siemens current emission data appears to correlate well with the ABB data. AS to send the data to FG.	AS
4.2	**Stage 1 & 2 Draft – Update** SPS has not made any changes to the draft text, pending agreement of the way forward for Figure 2, Figure 3 and Table 4.	

4.3	**Draft Fig 2 – New Analysis Spreadsheet** SPS explained the spreadsheet entitled: '61000-3-2 Further Analysis rev1'. This analysis looks at how many IEC 61000-3-2 compliant products, each emitting up to the Class A limits, can be connected for networks with reference impedance. Column G gives the voltage distortion created by one piece of equipment. Column K gives the maximum Global contribution from the LV, G_{hLV}, system taking account of the LV and HV planning levels - PL_{LV} and PL_{HV} - and assuming transfer from HV using a transfer coefficient, T, of 1.0 and summation exponent, α: $$G_{hLV} = \sqrt[\propto]{PL_{LV}{}^{\propto} - (T.PL_{HV})^{\propto}}$$ Column L gives G_{hLV} as a % of PL_{LV} calculated from the above equation. Column M gives the allocated G_{hLV} as a % of $PL_{LV,}$ notwithstanding the calculated G_{hLV}. Column N explains the basis of the allocated value where this differs from Column L. Columns R, T, V, X and Z give the voltage distortion for increasing number of items, N, from N=2 to N=6. Columns S, U, W, Y and AA give the comparison of the combined voltage distortion with the allocated $G_{hLV.}$ SPS showed the resulting revision to the draft Fig 2 Flow Chart, assuming one connection is allowed to use the whole allocated $G_{hLV.}$ 	

	SPS asked for any thoughts on how this could be improved. It was agreed that the values derived in this manner would be adopted provisionally for each connection rather than reduced to allow for multiple connections; it was agreed this was reasonable given that: i) The numbers permitted are small ii) The assumed position of the connections is lumped together at Zref – in reality, connections may be distributed, iii) Impedance could be less than Zref iv) Emissions could be lower than the maximum permitted by IEC 61000-3-2 v) Existing voltage distortion could serve to reduce emissions. vi) Failure of Stage 1A advances to Stage 1B and so on. SPS to proceed on the basis that the above is satisfactory and draft the text accordingly.	All SPS
4.4	**Draft Fig 3 – New Analysis Spreadsheet** SPS explained the spreadsheet entitled: '61000-3-12 Further Analysis rev1'. This analysis looks at the maximum equipment rating that satisfies a voltage change limit (phase-neutral) of 3% for reference impedance – see cell K4. It then uses that to derive current emission (Column B) for a single item of equipment. Column G gives the voltage distortion created by one such piece of equipment. Column K gives the maximum Global contribution from the LV, G_{hLV}, system taking account of the LV and HV planning levels - PL_{LV} and PL_{HV} - and assuming transfer from HV using a transfer coefficient, T, of 1.0 and summation exponent, α: $$G_{hLV} = \sqrt[\propto]{PL_{LV}{}^{\propto} - (T.PL_{HV})^{\propto}}$$ Column L gives G_{hLV} as a % of PL_{LV} calculated from the above equation. Column M gives the allocated G_{hLV} as a % of $PL_{LV,}$ notwithstanding the calculated G_{hLV}. Column N explains the basis of the allocated value where this differs from Column L. Columns R, T, V, X and Z give the voltage distortion for increasing number of items, N, from N=2 to N=6. Columns S, U, W, Y and AA give the comparison of the combined voltage distortion with the allocated $G_{hLV.}$ SPS showed the resulting revision to the draft Fig 3 Flow Chart, assuming one connection is allowed to use the whole allocated $G_{hLV.}$	



SPS explained that this needs to be further improved to permit larger numbers of devices with smaller equipment ratings (down to 16A).

SPS showed work started on looking at the required short-circuit fault level to replace Table 4a and 4b. This is based on the same assumptions as above fort Figure 3.

	A	B	C	D	E	F	G
1	**Phases**	3					
2	**Service Current Capacity**	<100A					
3							
4		**$S_{SC\ MIN}$ (VA)**					
5	**I_{equ} (A)**	N=1	N=2	N=3	N=4	N=5	N=6
6	**16**	252220	356692	440816	541377	634923	723234
7	**20**	315274	445865	551020	676721	793653	904043
8	**25**	394097	557332	688775	845901	992067	1130053
9	**30**	472912	668798	826530	1015081	1190480	1356064
10	**35**	551730	780264	964285	1184261	1388894	1582075
11	**40**	630549	891731	1102040	1353441	1587307	1808085
12	**45**	709367	1003197	1239795	1522622	1785720	2034096
13	**50**	788186	1114663	1377551	1691802	1984134	2260107
14	**55**	867005	1226130	1515306	1860982	2182547	2486117
15	**60**	945823	1337596	1653061	2030162	2380960	2712128
16	**65**	1024642	1449062	1790816	2199342	2579374	2938139
17	**70**	1103461	1560529	1928571	2368523	2777787	3164150
18	**75**	1182279	1671995	2066326	2537703	2976201	3390160

The orange cells show cases where the minimum fault level values are lower than the fault level associated with the reference impedance. These could replace the decision '≤2 items, each with Iequ ≤24.4A'. The table could be refined to show 1A increments.

	SPS showed a spreadsheet entitled 'SSC MIN CALC'. SPS is to use this to explore whether a minimum S_{SC} statement by a manufacturer, applicable when the Rsce =33 limits are not met, can be applied as it stands or if some correction is required given the different assumptions underpinning the limits in IEC 61000-3-12 than those proposed to be used above. Initial indications were that ensuring Rsce = 33 would suffice. The issue of multiple devices on the same connection each with a required S_{SC} was discussed. It was agreed that a simple approach would be to increase the required fault level by multiplying the stated required S_{SC} by the number of items. SPS to consider further and revise the draft accordingly.	SPS
4.5	**Stage 2C – Impact of 77A/926/CDV Compatibility Levels beyond 40th** SPS showed the group the interim response from FGh/BG: 'We think that accepting the IEC document as the basis for compatibility levels would avoid a lot of discussions later. However, we need to understand exactly how the proposed CP can be used and what the implications would be. We would come back to you with our final proposal but as things stand now we probably recommend the use of IEC.'	FGh/ BG
4.6	**Stage 1 & 2 Draft Worked Examples - Update** SPS has not made any changes to the draft text, pending agreement of the way forward for Figure 2, Figure 3 and Table 4 (and treatment of harmonics above the 40th for Stage 2C).	
4.7	**Stage 2C Thevenin Equivalent Example** FG showed how the current emission in the face of pre-existing background voltage distortion can be deduced via an iterative process using ABB Drive Size software. It was recognised that the example we include in the Worked Examples must not be manufacturer specific. It was agreed that FG would prepare a simple worked example based on superposition to illustrate how to take advantage of the reduced current emission that occurs when background voltage distortion is considered. It was noted that it might be possible to give advice in a Note to the draft Stage 2C text that indicates when the above effect would make a material change to the emissions (e.g. by advising on the ratio of internal to external impedance); FG to consider.	FG FG
5	**Agree Further Work** See the actions recorded above.	
6	**AOB** None.	
7	**Future meetings** • Dates	

	The date of the next meeting was agreed as **11 January 2016**. Venue to be arranged by AS if a room can be found at Siemens, Manchester. • Agenda items Not discussed.	AS SPS